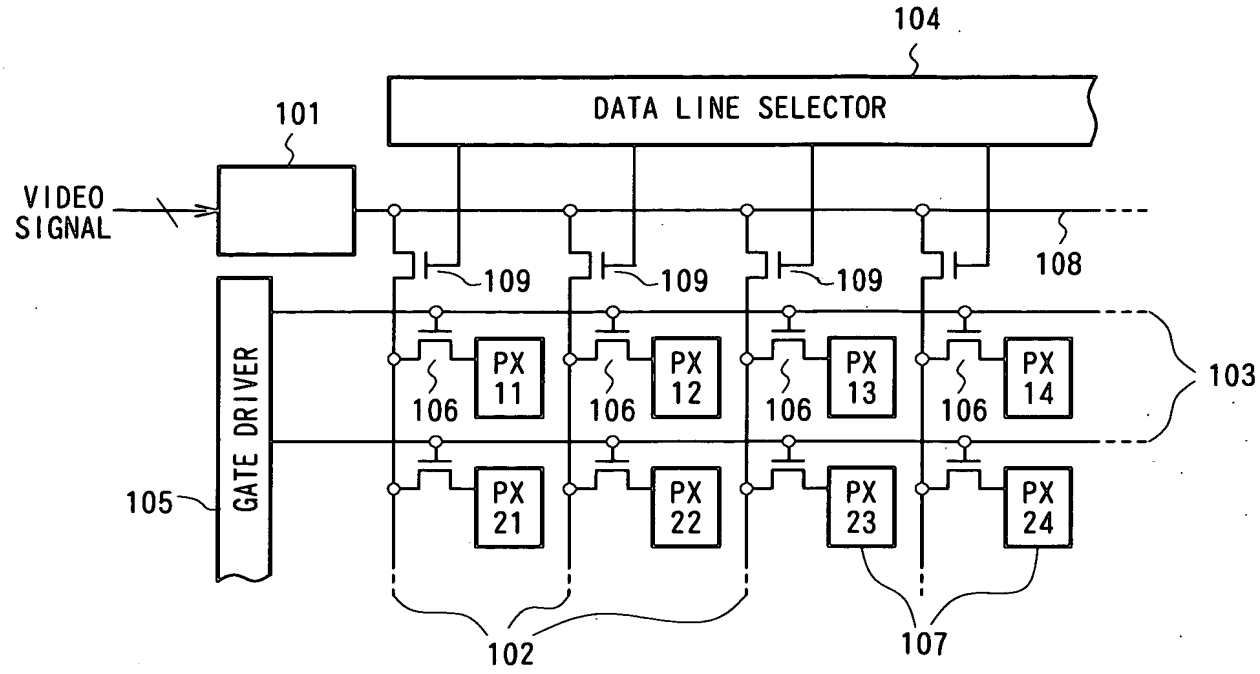

Fig. 1 PRIOR ART

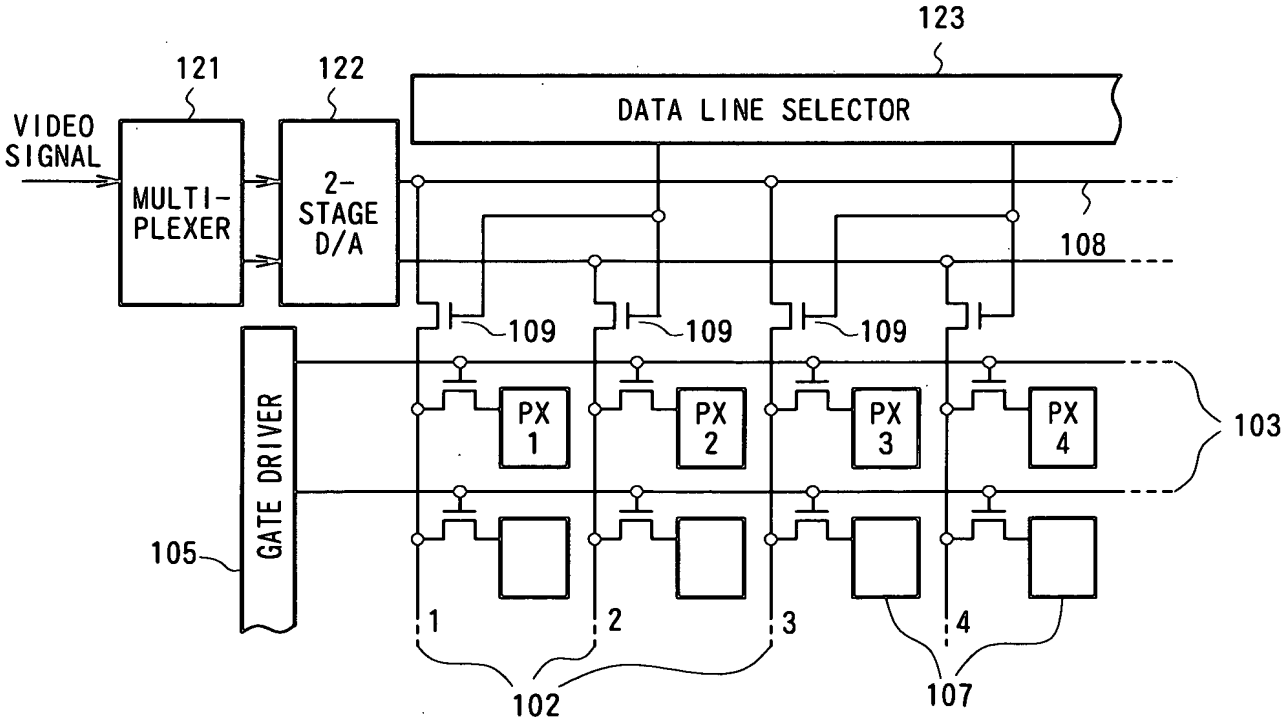

Fig. 2 PRIOR ART

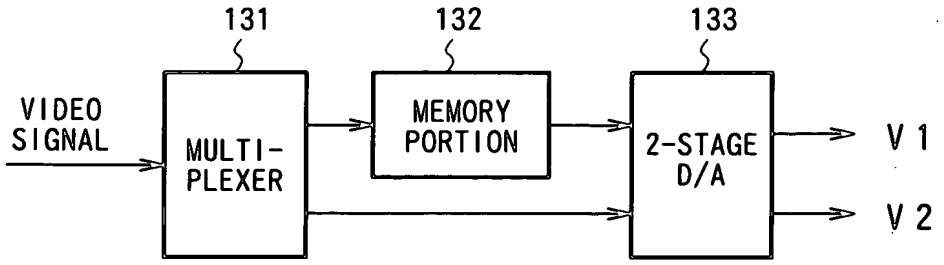

Fig. 3A PRIOR ART

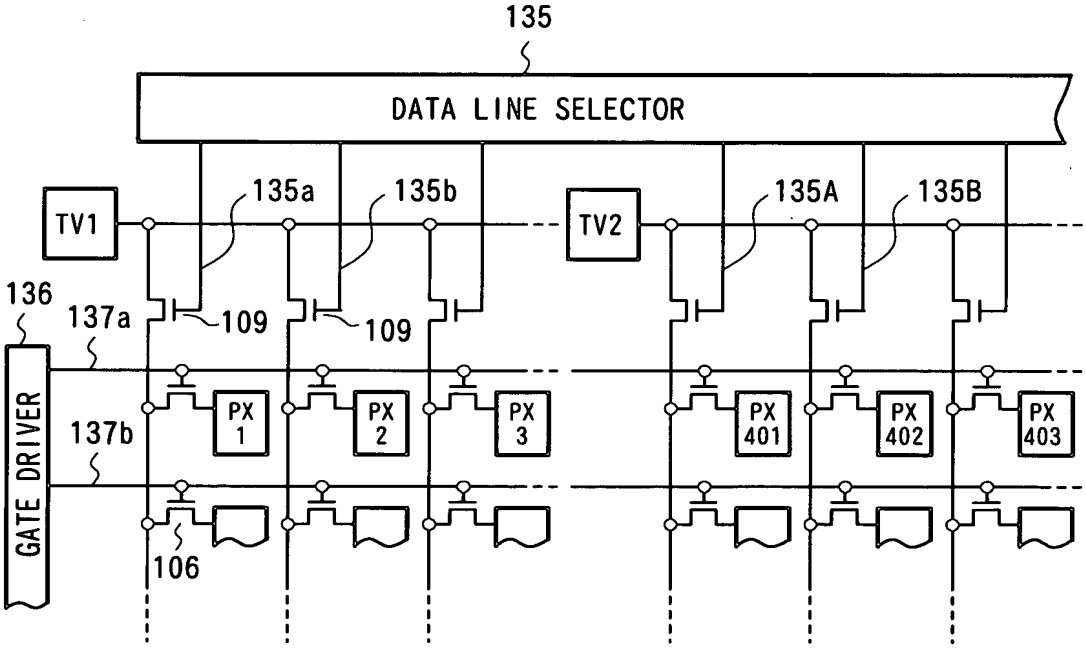

Fig. 3B PRIOR ART

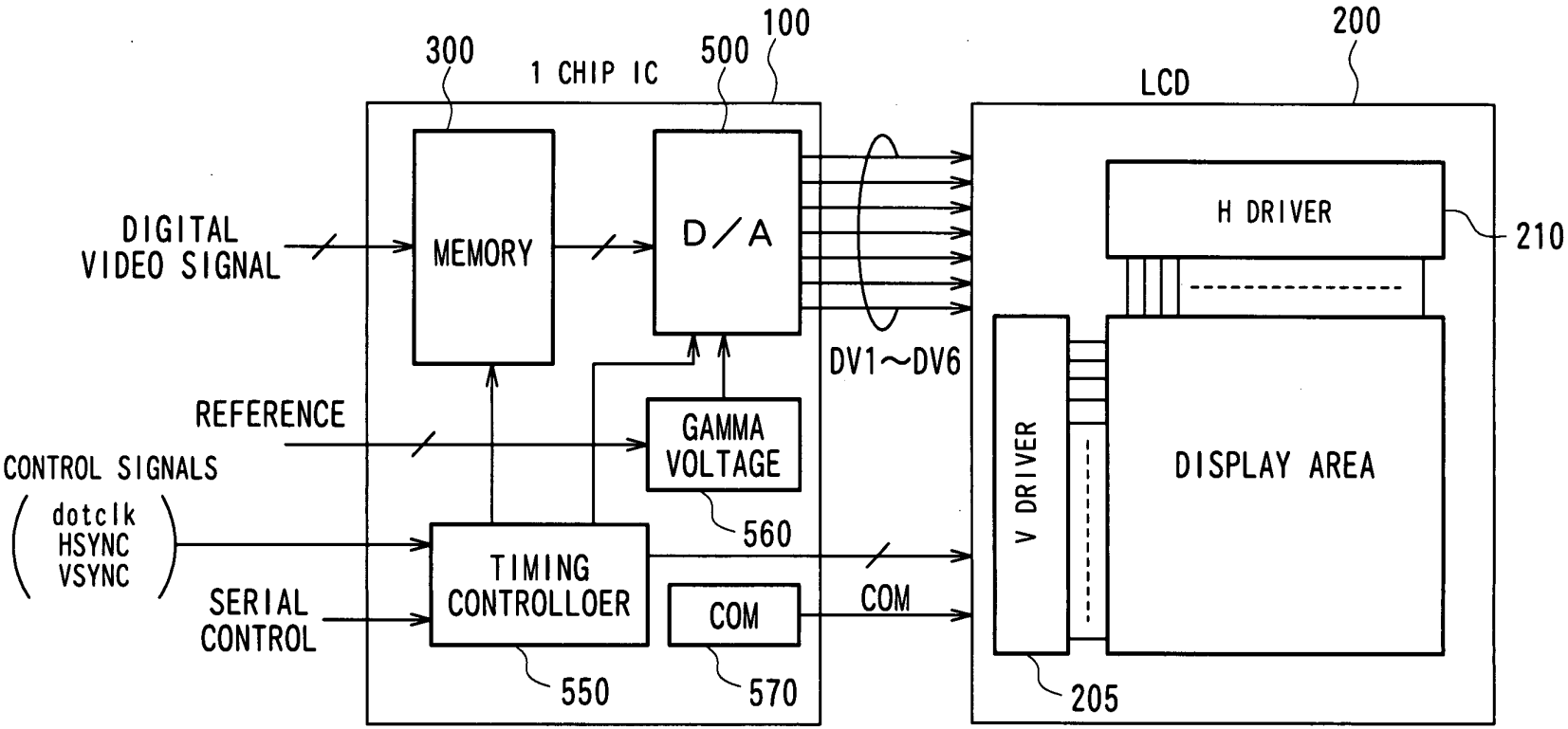
300
1 CHIP IC
500
100
200
LCD
DIGITAL
VIDEO SIGNAL
MEMORY
D/A
H DRIVER
210
DV1~DV6
REFERENCE
GAMMA
VOLTAGE
CONTROL SIGNALS
dotclk
HSYNC
VSYNC
560
TIMING
CONTROLLOER
COM
COM
SERIAL
CONTROL
V DRIVER
DISPLAY AREA
550
570
205

Fig. 4

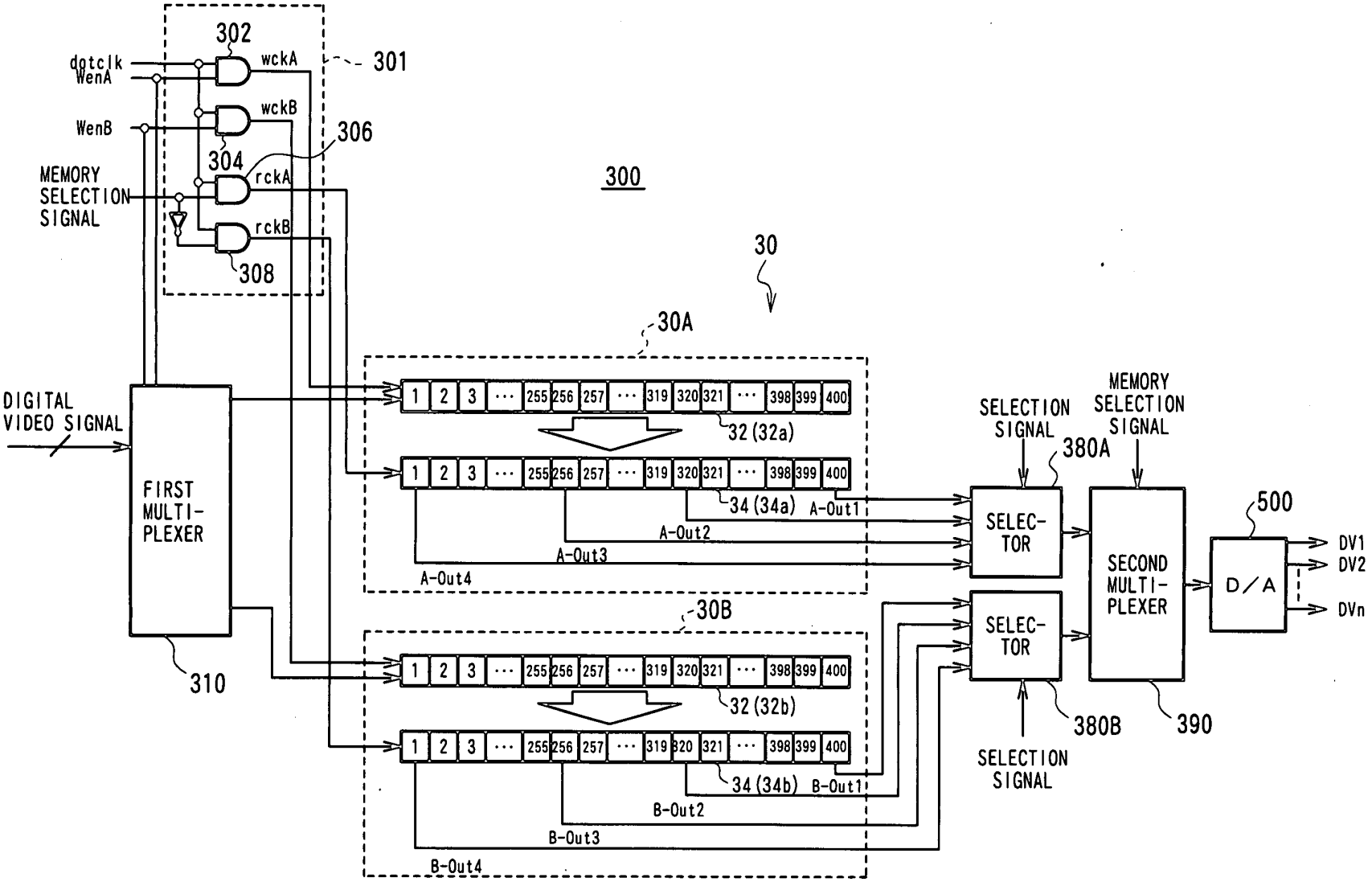
300
30
30A
30B
302
301
306
304
308
dotclk
WenA
WenB
MEMORY SELECTION SIGNAL
wckA
wckB
rckA
rckB
DIGITAL VIDEO SIGNAL
FIRST MULTI-PLEXER
310
1 2 3 ··· 255 256 257 ··· 319 320 321 ··· 398 399 400
32 (32a)
34 (34a)
A-Out1
A-Out2
A-Out3
A-Out4
32 (32b)
34 (34b)
B-Out1
B-Out2
B-Out3
B-Out4
SELECTION SIGNAL
380A
MEMORY SELECTION SIGNAL
SELEC-TOR
SECOND MULTI-PLEXER
380B
390
500
D/A
DV1
DV2
DVn

Fig. 5

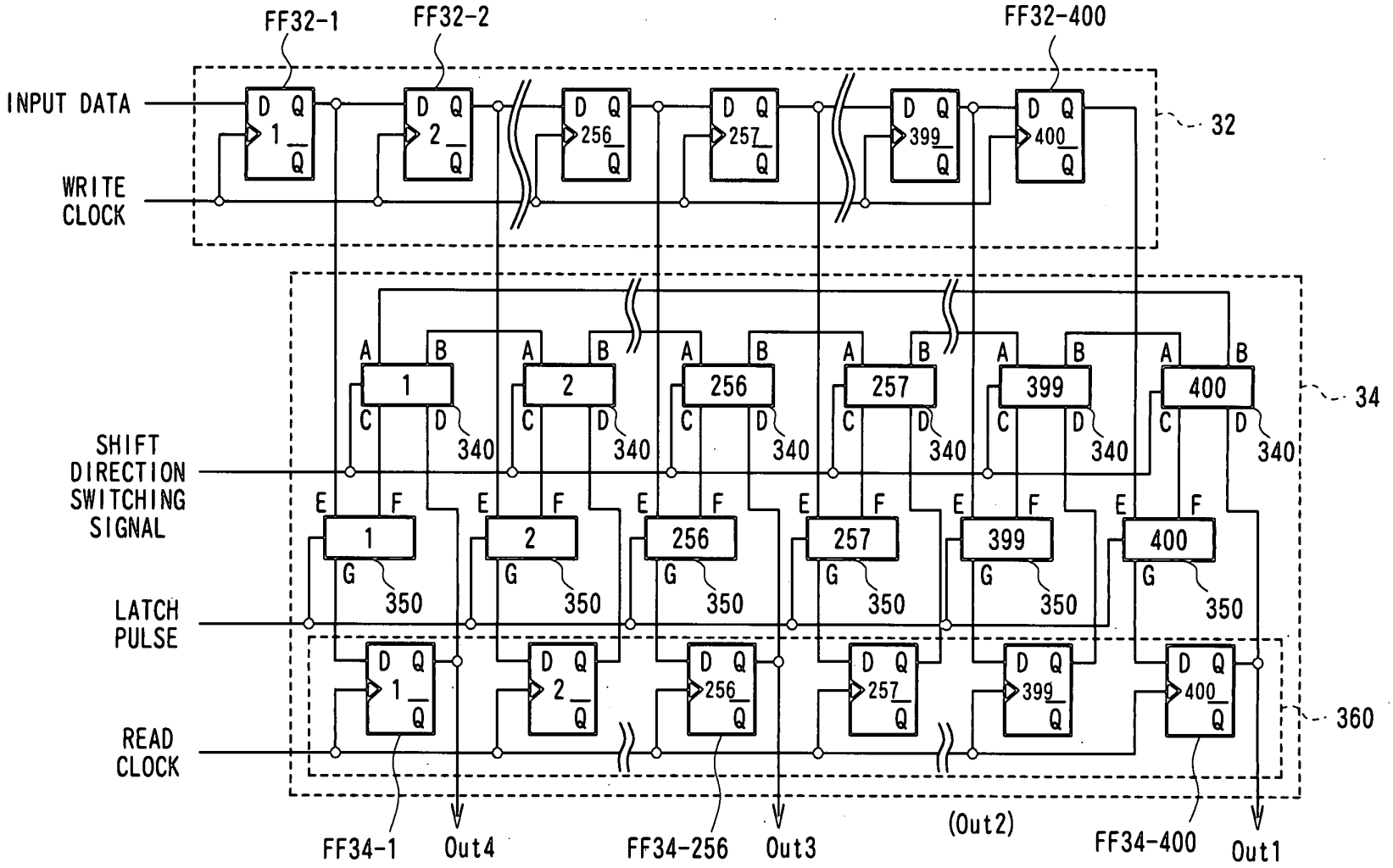
FF32-1
FF32-2
FF32-400
INPUT DATA
WRITE CLOCK
32
34
SHIFT DIRECTION SWITCHING SIGNAL
LATCH PULSE
READ CLOCK
360
340
350
FF34-1
Out4
FF34-256
Out3
(Out2)
FF34-400
Out1

Fig. 6A

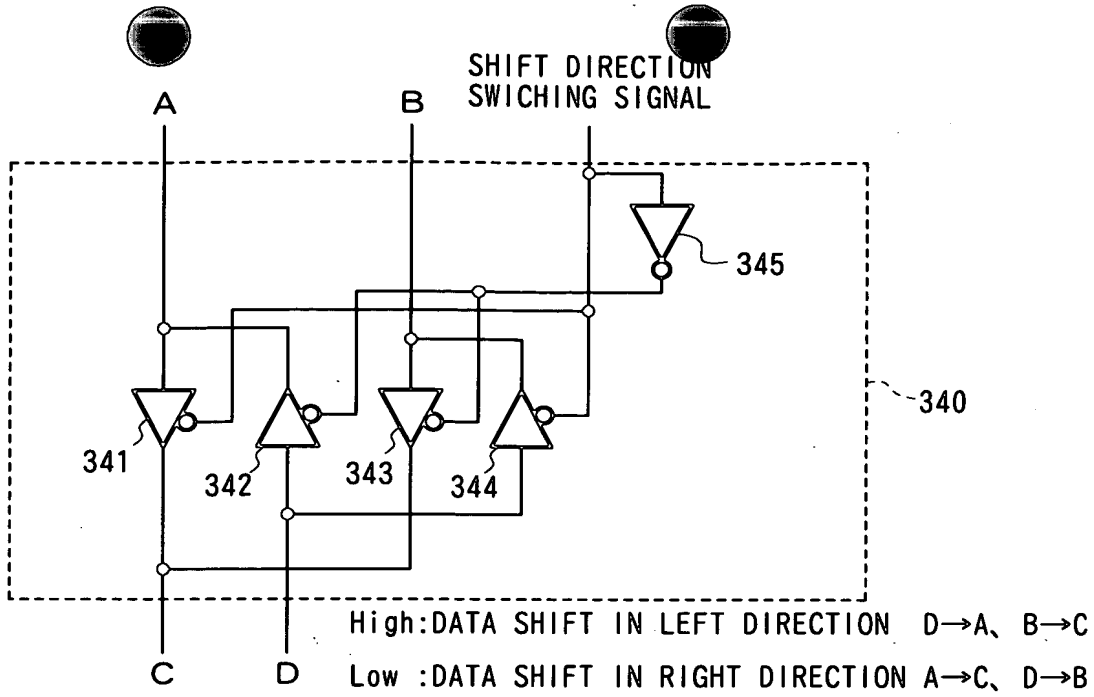

Fig. 6B

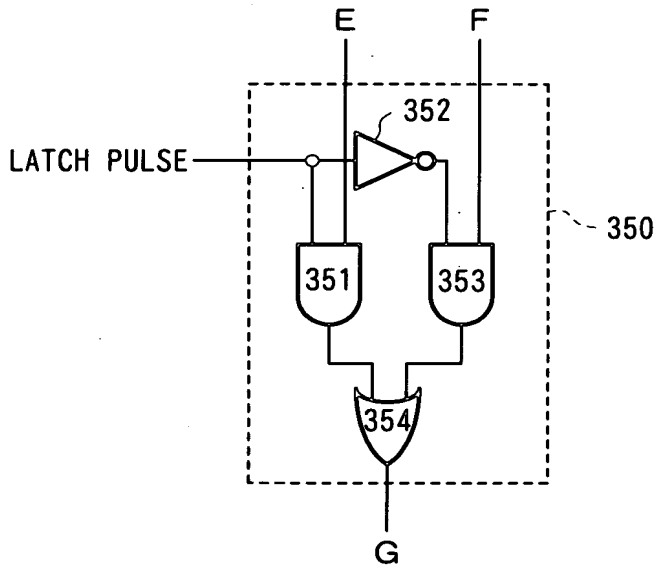

Fig. 6C

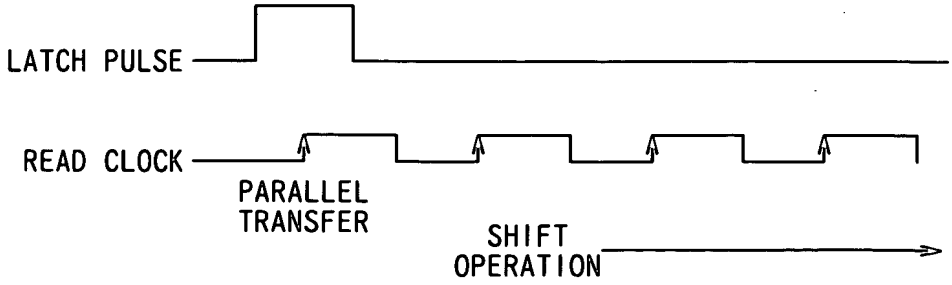

Fig. 6D

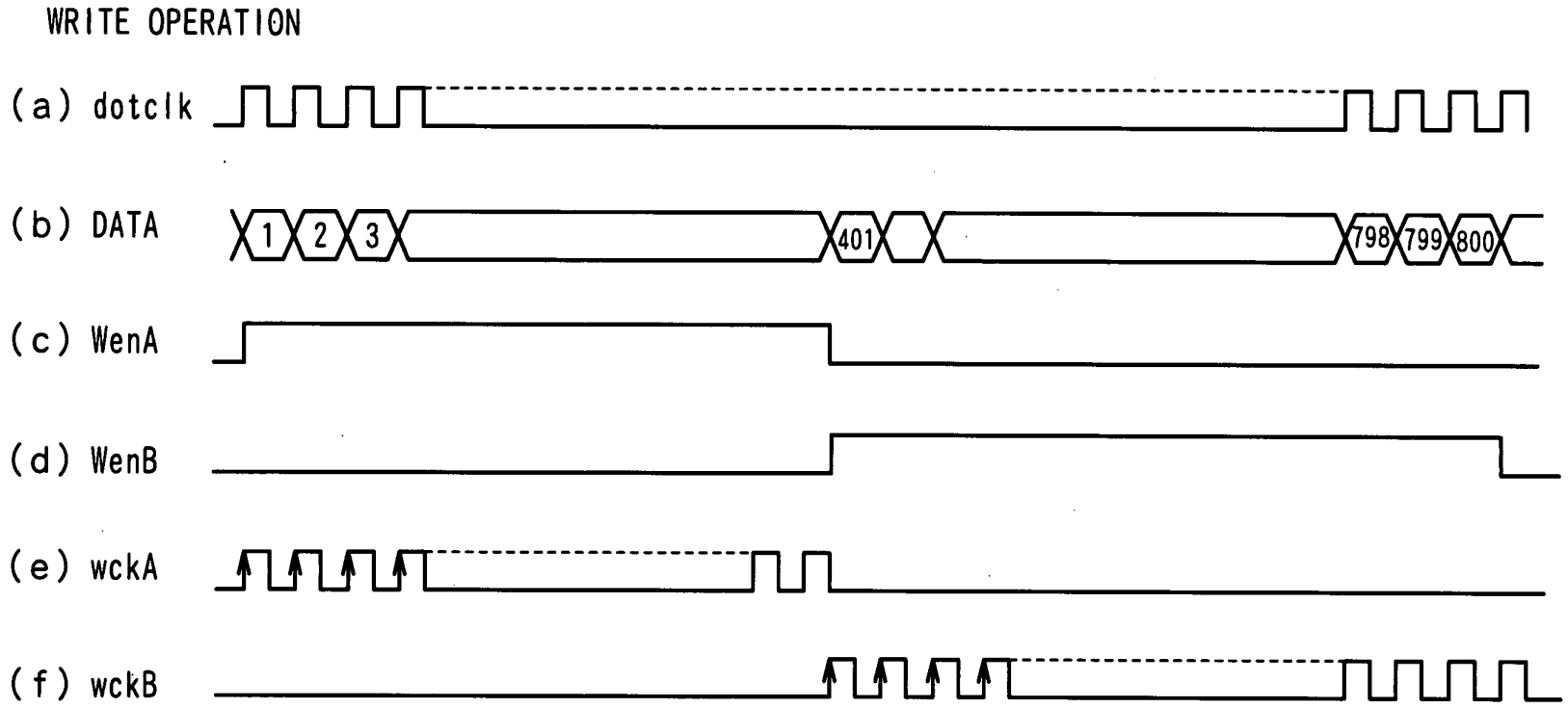
WRITE OPERATION
(a) dotclk
(b) DATA
1
2
3
401
798
799
800
(c) WenA
(d) WenB
(e) wckA
(f) wckB

Fig. 7

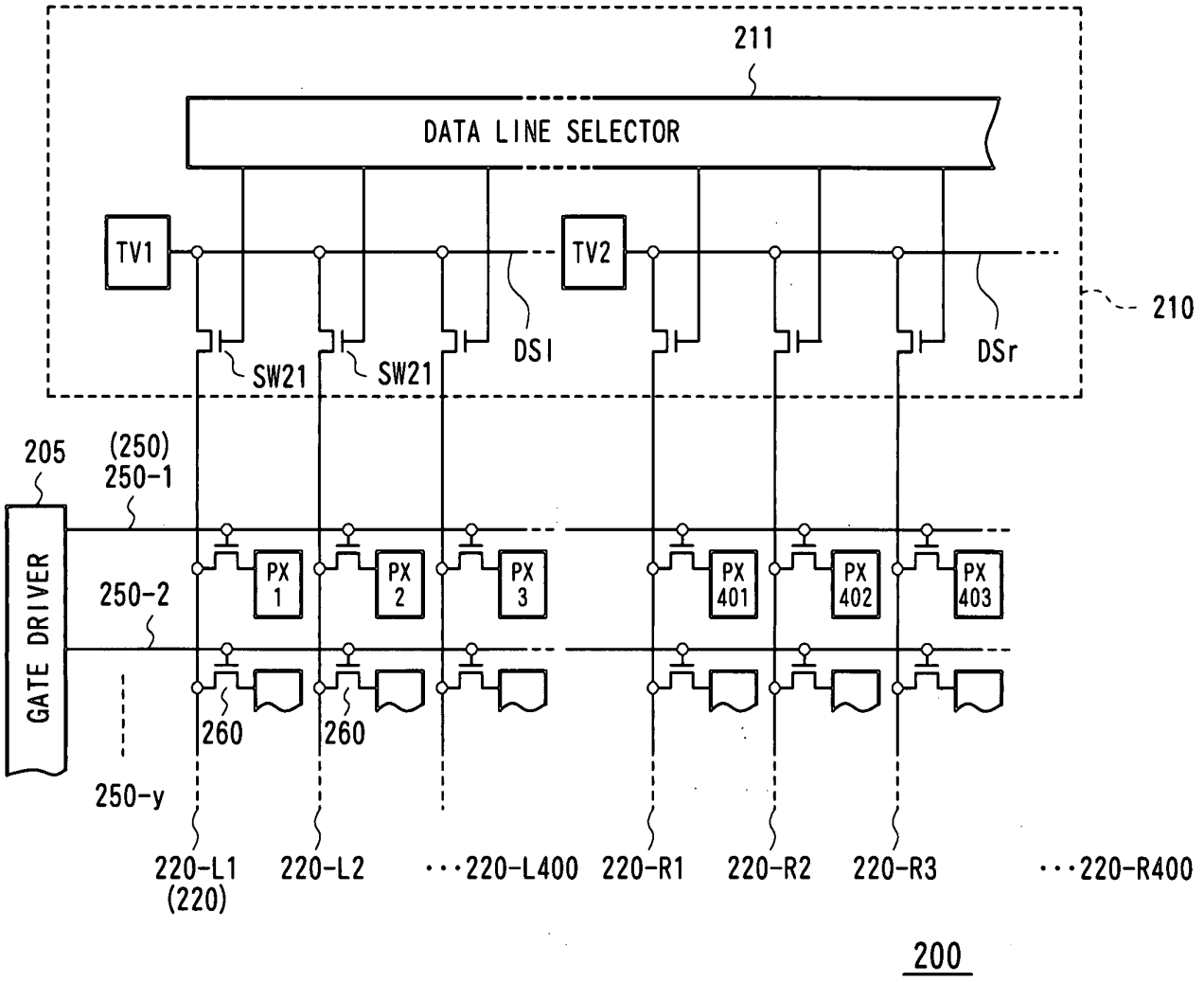

Fig. 8

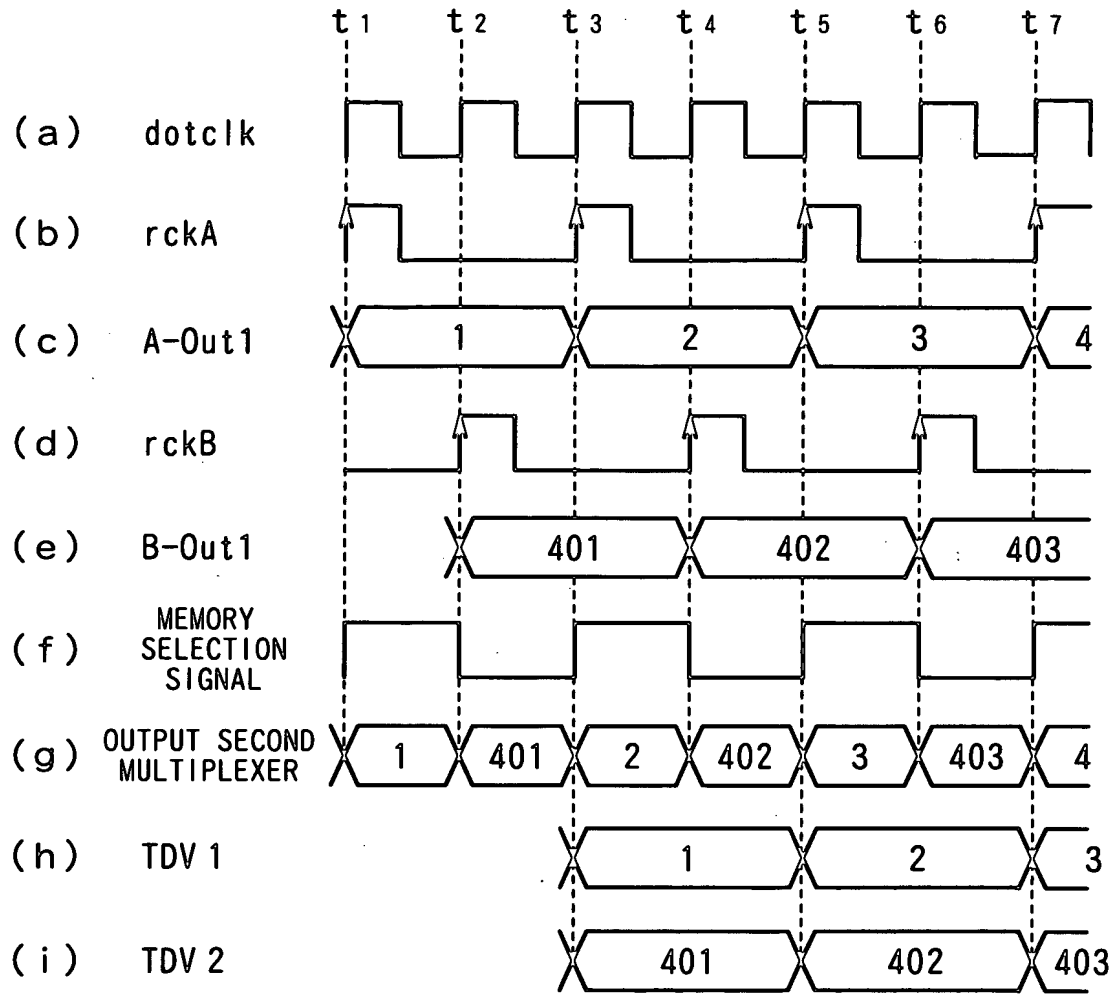
t1
t2
t3
t4
t5
t6
t7
(a) dotclk
(b) rckA
(c) A-Out1
1
2
3
4
(d) rckB
(e) B-Out1
401
402
403
(f) MEMORY SELECTION SIGNAL
(g) OUTPUT SECOND MULTIPLEXER
1
401
2
402
3
403
4
(h) TDV 1
1
2
3
(i) TDV 2
401
402
403

Fig. 9

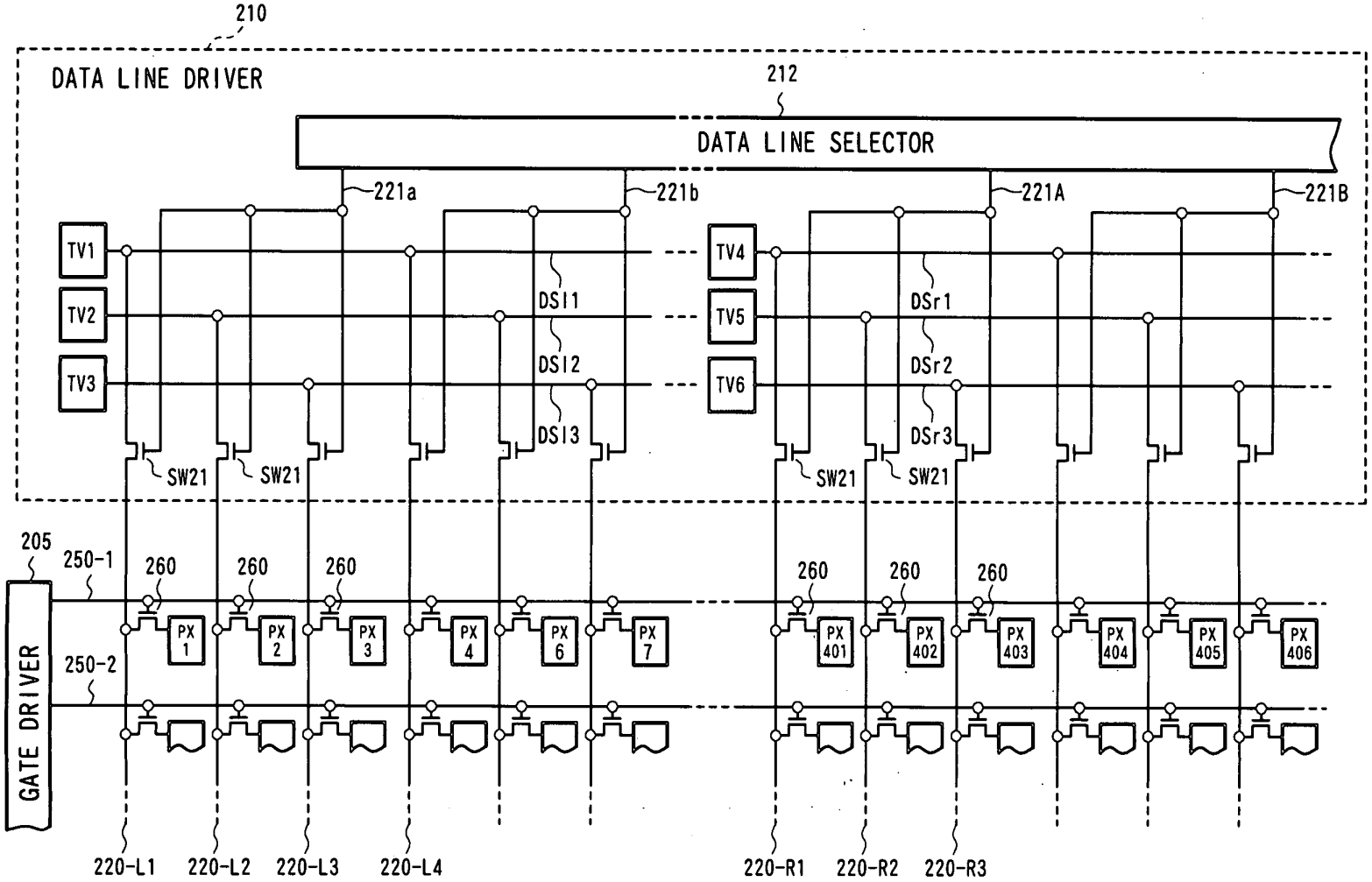
210
DATA LINE DRIVER
212
DATA LINE SELECTOR
221a
221b
221A
221B
TV1
TV2
TV3
TV4
TV5
TV6
DSl1
DSl2
DSl3
DSr1
DSr2
DSr3
SW21
205
GATE DRIVER
250-1
250-2
260
PX 1
PX 2
PX 3
PX 4
PX 6
PX 7
PX 401
PX 402
PX 403
PX 404
PX 405
PX 406
220-L1
220-L2
220-L3
220-L4
220-R1
220-R2
220-R3

Fig. 10

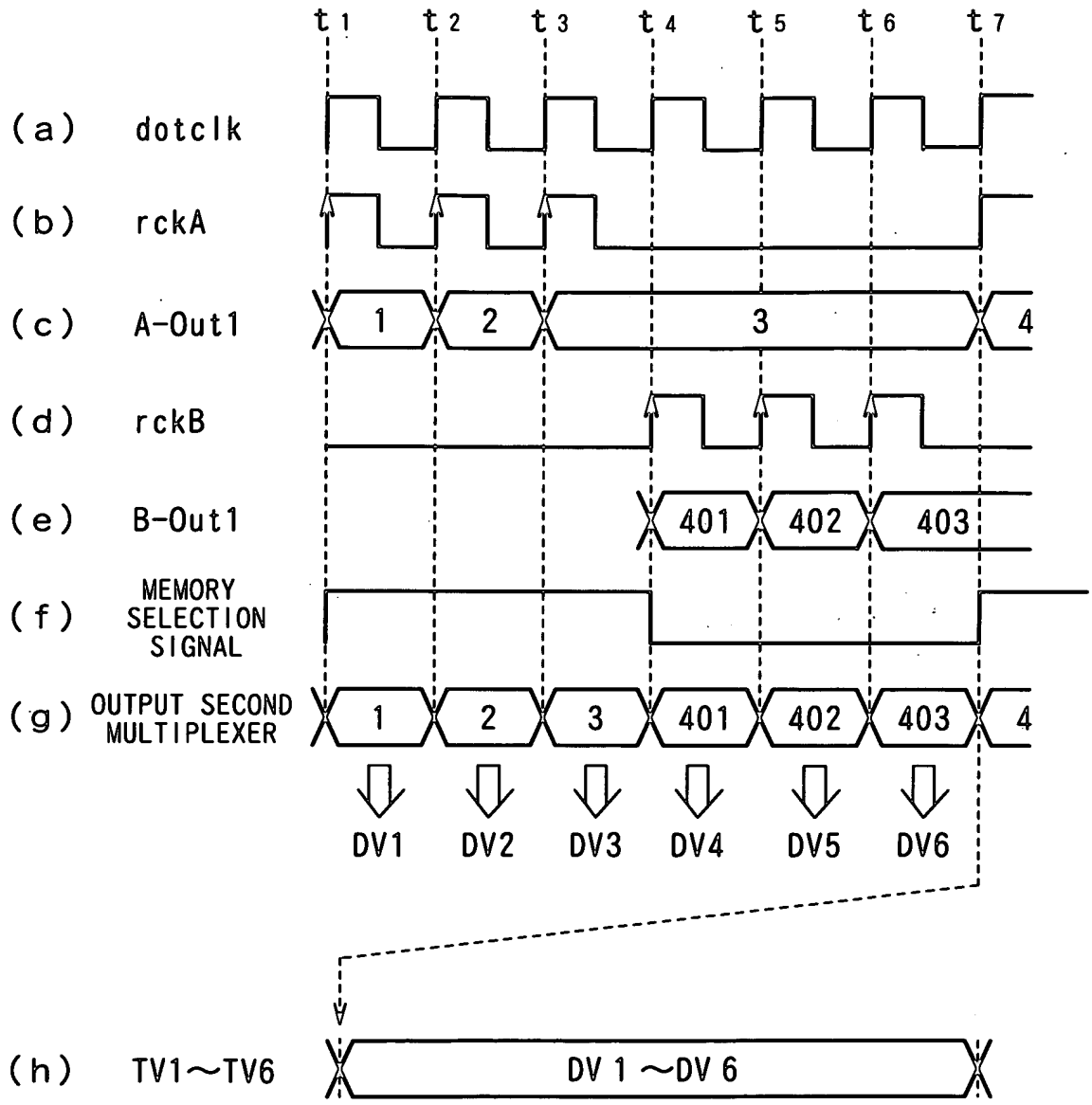
t1
t2
t3
t4
t5
t6
t7
(a) dotclk
(b) rckA
(c) A-Out1
1
2
3
4
(d) rckB
(e) B-Out1
401
402
403
(f) MEMORY SELECTION SIGNAL
(g) OUTPUT SECOND MULTIPLEXER
1
2
3
401
402
403
4
DV1
DV2
DV3
DV4
DV5
DV6
(h) TV1～TV6
DV 1 ～DV 6

Fig. 11

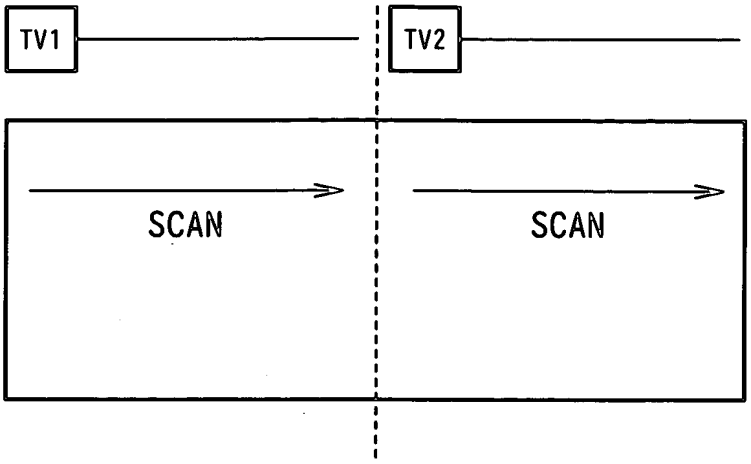

Fig. 12A

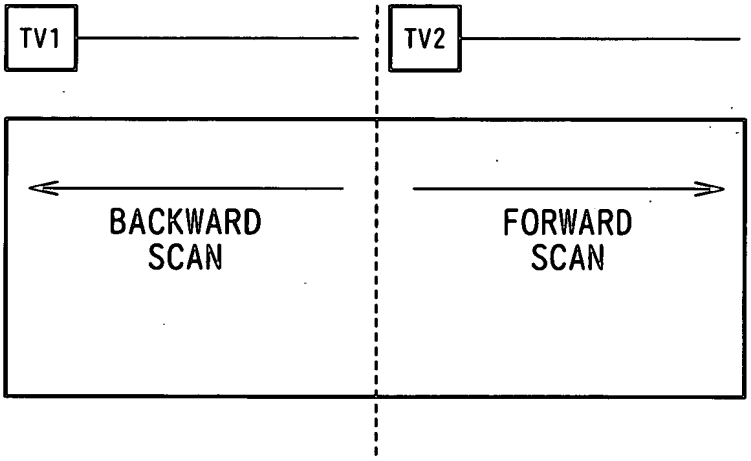

Fig. 12B

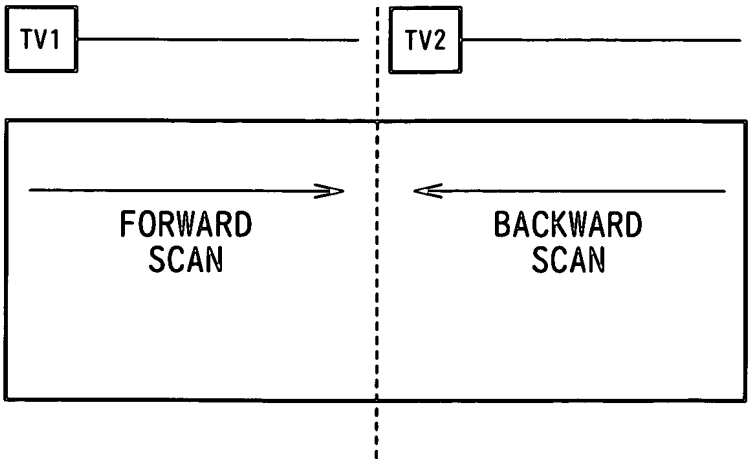

Fig. 12C

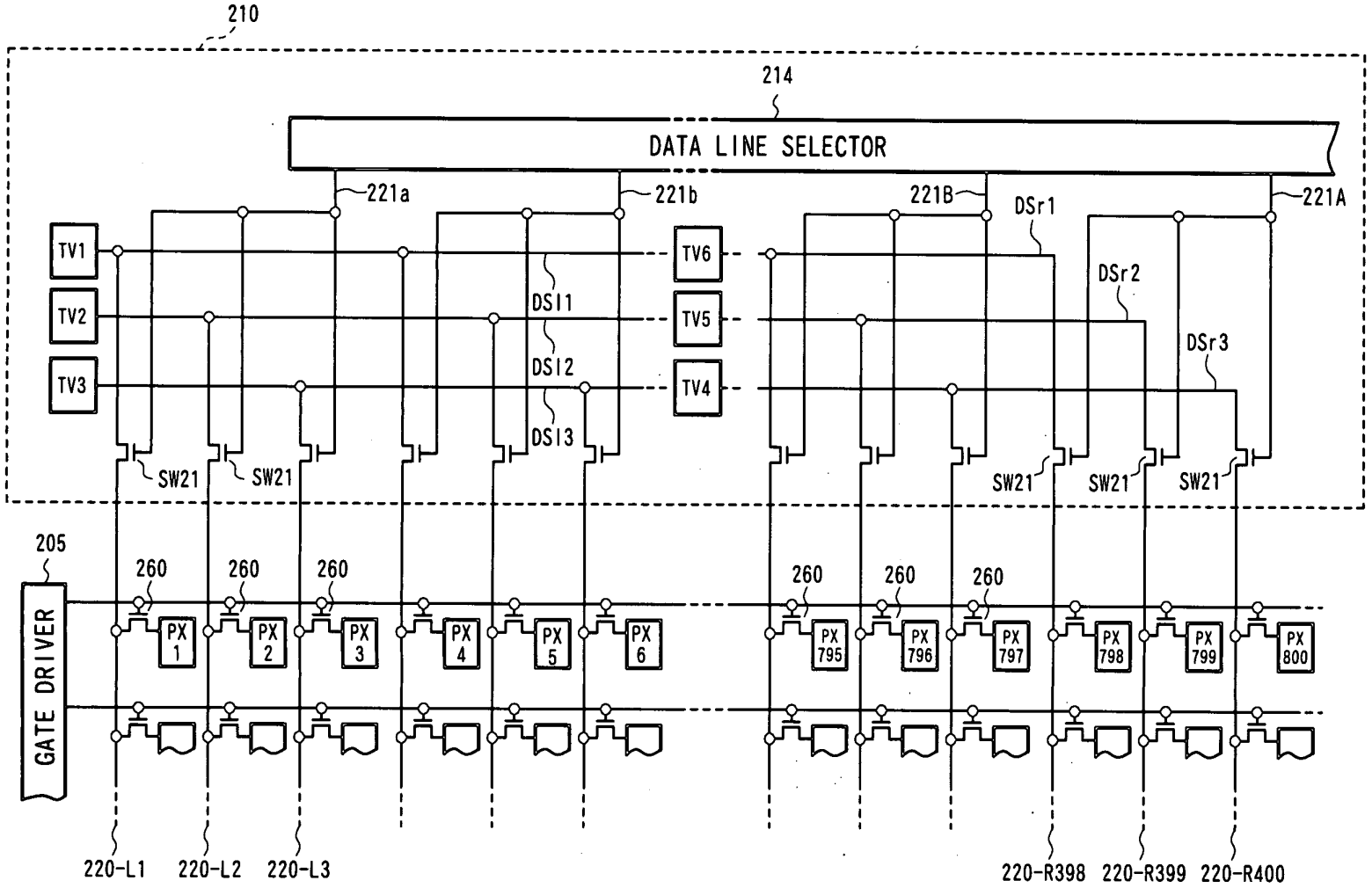
210
214
DATA LINE SELECTOR
221a
221b
221B
221A
DSr1
DSr2
DSr3
TV1
TV2
TV3
TV4
TV5
TV6
DSl1
DSl2
DSl3
SW21
205
GATE DRIVER
260
PX 1
PX 2
PX 3
PX 4
PX 5
PX 6
PX 795
PX 796
PX 797
PX 798
PX 799
PX 800
220-L1
220-L2
220-L3
220-R398
220-R399
220-R400

Fig. 13

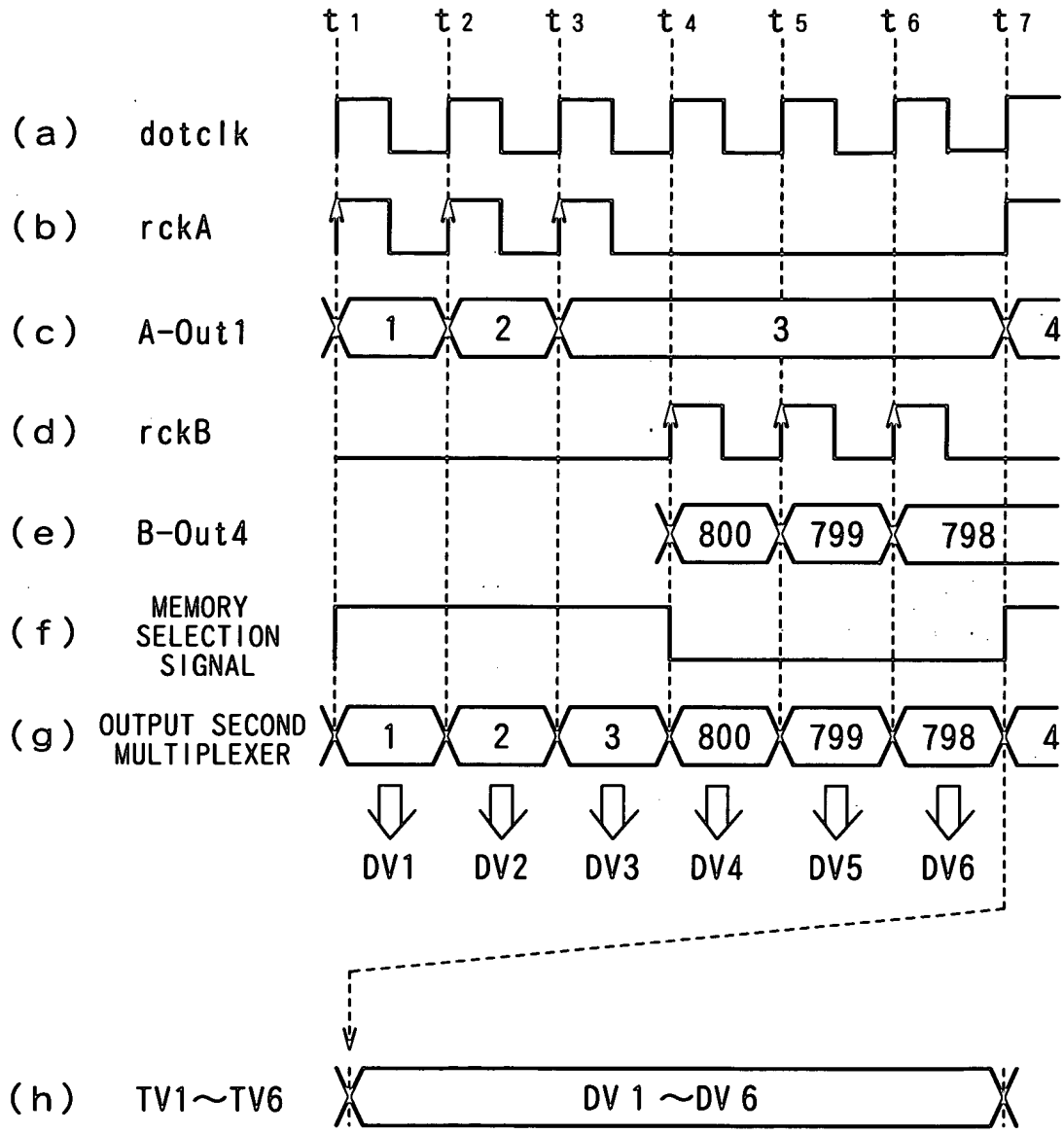
t1
t2
t3
t4
t5
t6
t7
(a) dotclk
(b) rckA
(c) A-Out1
1
2
3
4
(d) rckB
(e) B-Out4
800
799
798
(f) MEMORY SELECTION SIGNAL
(g) OUTPUT SECOND MULTIPLEXER
1
2
3
800
799
798
4
DV1
DV2
DV3
DV4
DV5
DV6
(h) TV1～TV6
DV 1 ～DV 6

Fig. 14

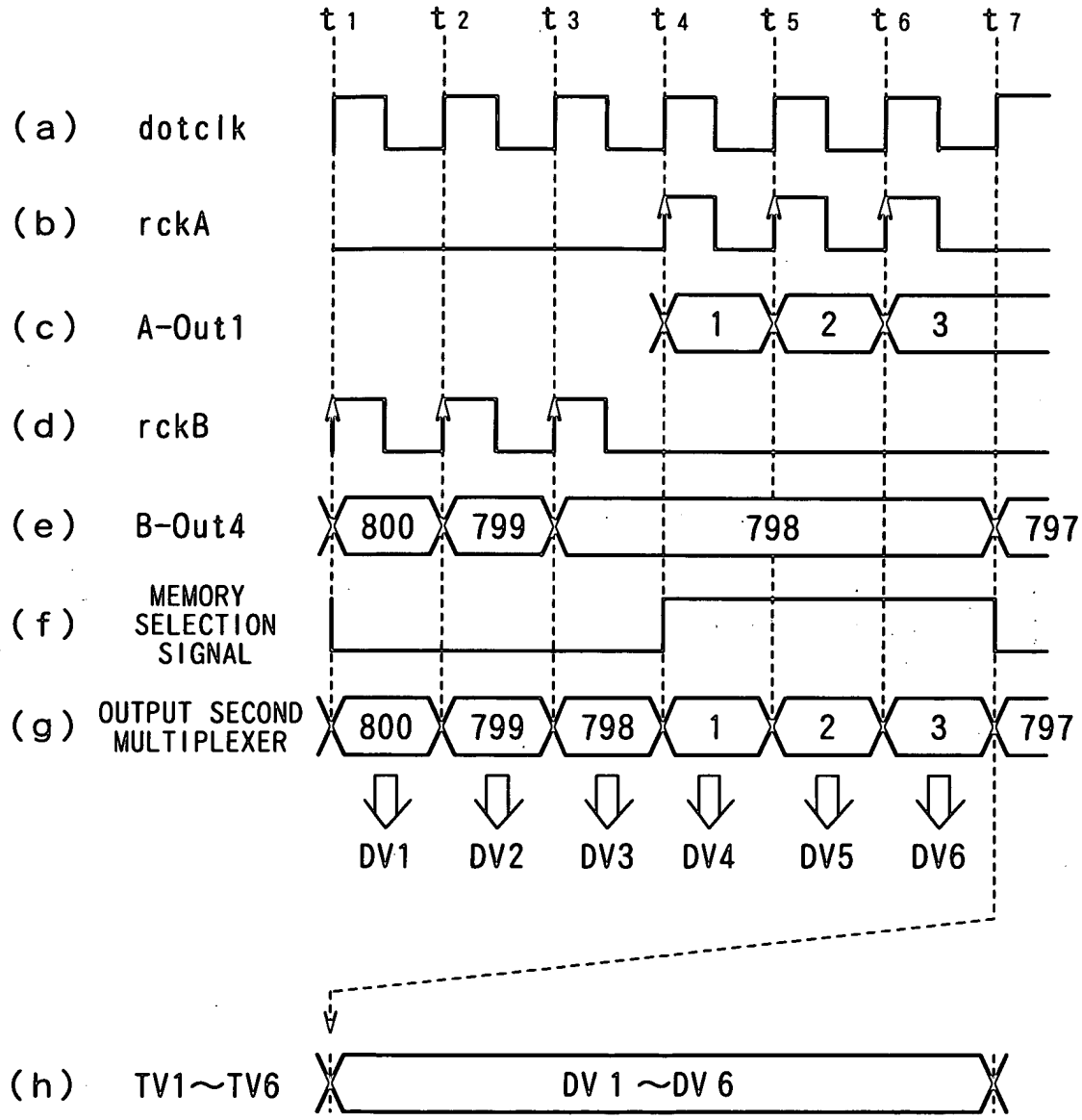
t1
t2
t3
t4
t5
t6
t7
(a) dotclk
(b) rckA
(c) A-Out1
1
2
3
(d) rckB
(e) B-Out4
800
799
798
797
(f) MEMORY SELECTION SIGNAL
(g) OUTPUT SECOND MULTIPLEXER
800
799
798
1
2
3
797
DV1
DV2
DV3
DV4
DV5
DV6
(h) TV1～TV6
DV 1 ～DV 6

Fig. 15

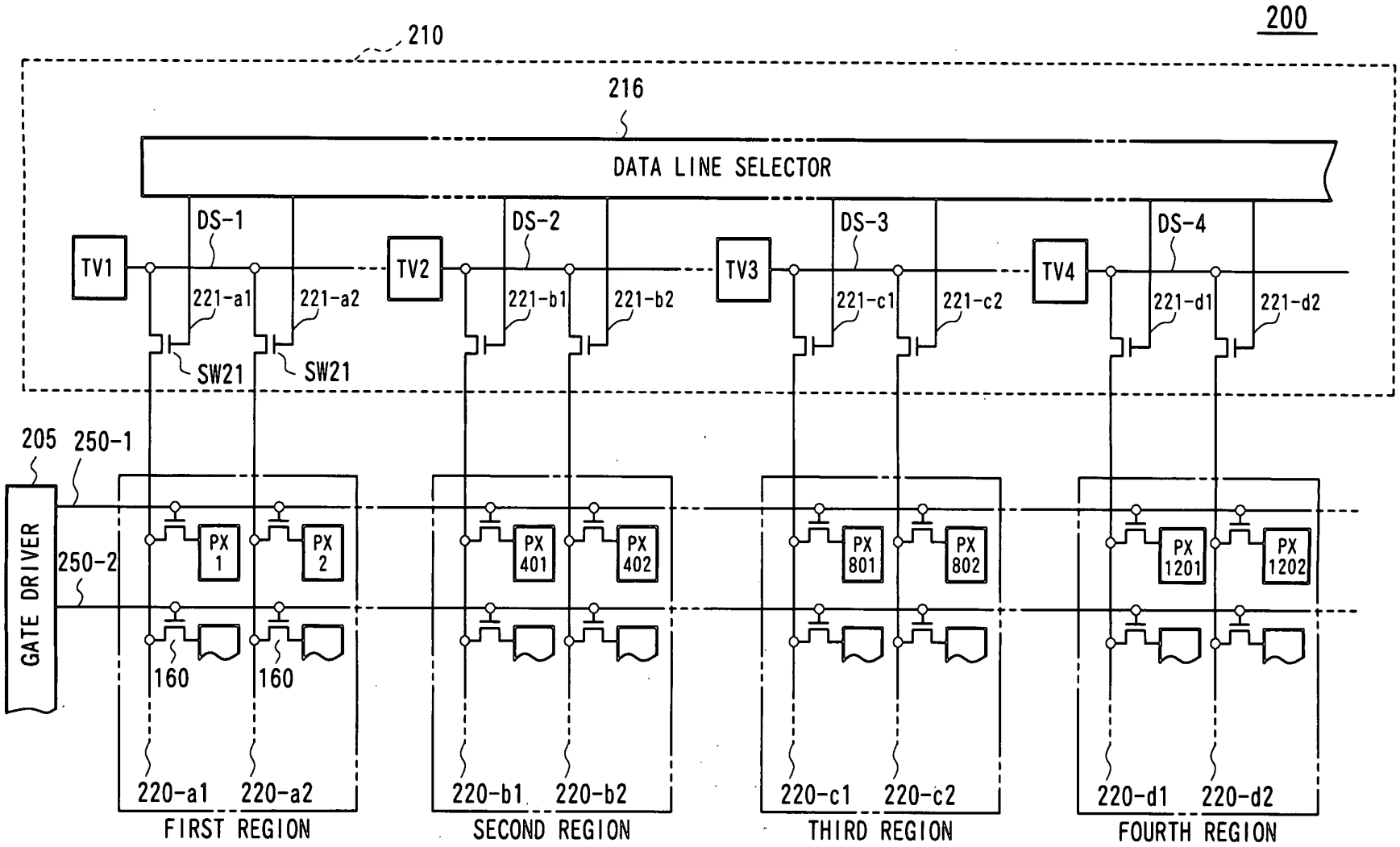
200
210
216
DATA LINE SELECTOR
DS-1
DS-2
DS-3
DS-4
TV1
TV2
TV3
TV4
221-a1
221-a2
221-b1
221-b2
221-c1
221-c2
221-d1
221-d2
SW21
SW21
205
250-1
250-2
GATE DRIVER
PX 1
PX 2
PX 401
PX 402
PX 801
PX 802
PX 1201
PX 1202
160
160
220-a1
220-a2
220-b1
220-b2
220-c1
220-c2
220-d1
220-d2
FIRST REGION
SECOND REGION
THIRD REGION
FOURTH REGION

Fig. 16

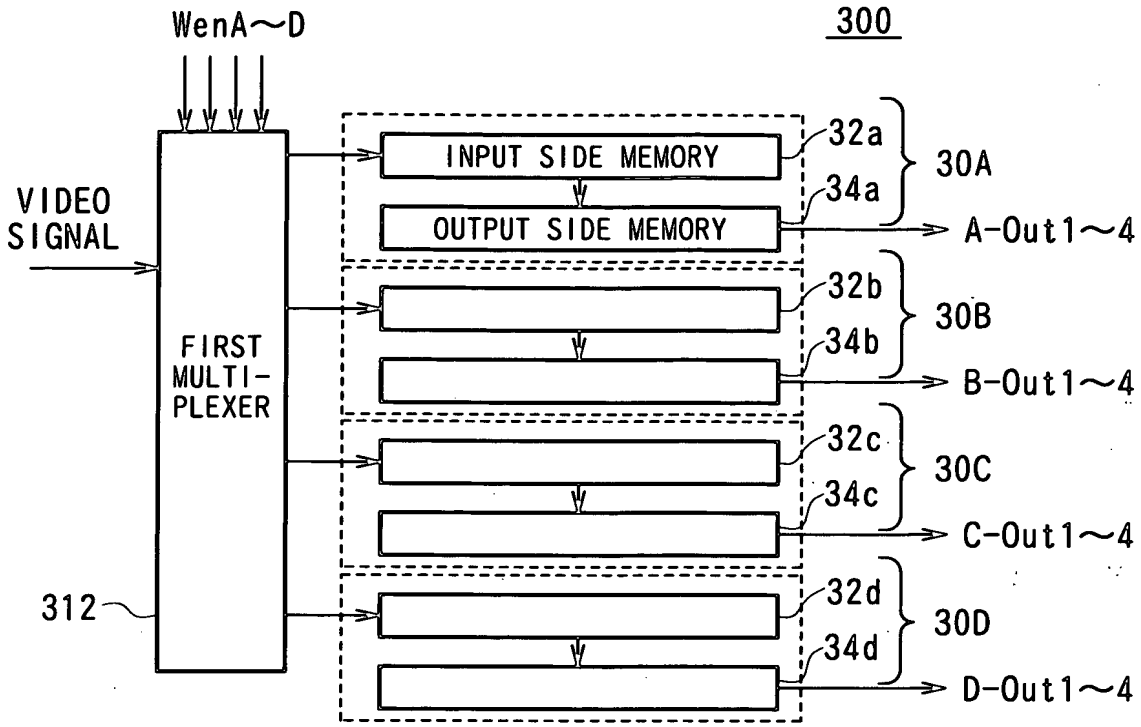

Fig. 17A

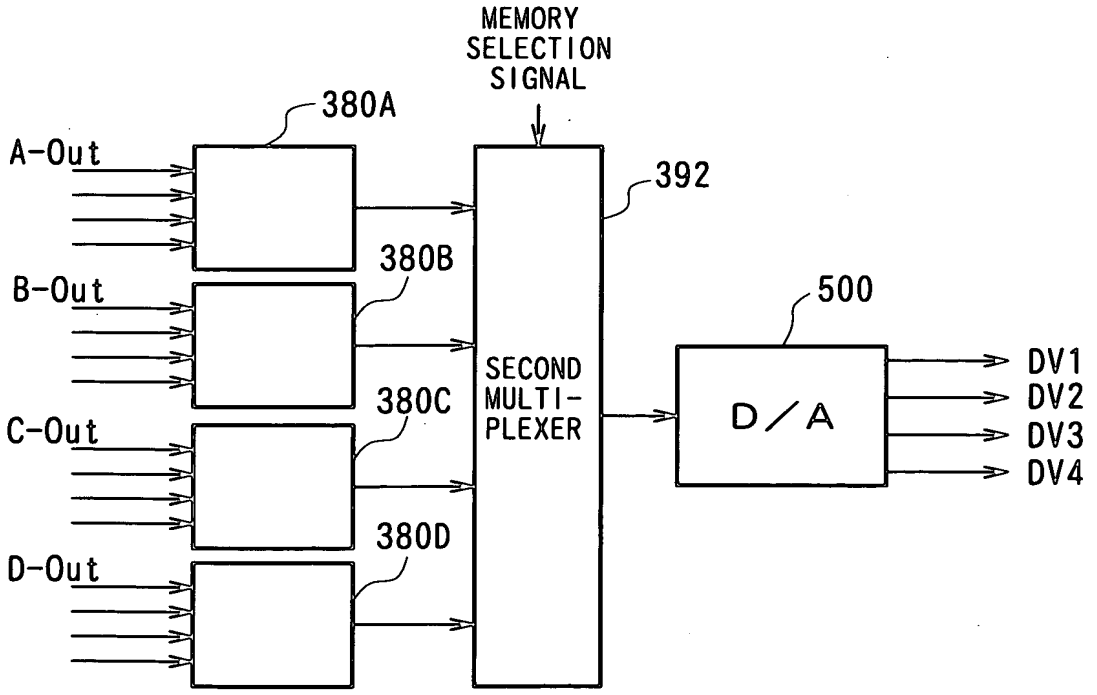

Fig. 17B